

IN THE SPECIFICATION

Paragraph starting at page 8, line 5:

As shown in Fig. 3, the comparator 204-2 comprises nineteen transistors Q302, Q304, Q306, Q308, Q310, Q312, Q314, Q316, Q318, Q320, Q322, Q324, Q326, Q328, Q330, Q332, Q334, Q336 and Q338. The source terminal of the transistor Q304 receives the digital signal SD. The source terminal of the transistor Q302 receives the reference voltage V_{ref} . The signal SR_out2 [[1]] is input to the gate terminals of the transistors Q302, Q304 and Q316. The signal SR_out3 [[2]] is input to the gate terminals of the transistors Q306, Q322 and Q328. The gate terminal of the transistor Q318 receives a signal SR_out1 [[0]]. The signal SR_out1 [[0]] is generated from the horizontal shift register 222 to control the comparator 204-1. Power is supplied to the source terminals of the transistors Q316, Q324, Q330, Q334 and Q338. The source terminals of the transistors Q306, Q320, Q326, Q332, Q336 and Q338 are coupled to a common electrode (in the embodiment, to ground).

Paragraph starting at page 10, line 13:

Fig. 5 is a timing diagram illustrating signals in Fig. 2, Fig. 3 and Fig. 4. The vertical axis is amplitude. The horizontal axis is time. Line 50 is the digital signal SD input to the compactor. Line 52 is the signal SR_out2 [[1]] generated from the horizontal shift register 222. Line 54 is a signal stored in the Latch 430.

Paragraph starting at page 10, line 19:

When the signal SR_out2 [[1]] generated from the horizontal shift register 222 first turns on, the digital signal SD (1) is input to the compactor. After comparison with the reference voltage, the digital signal “1” is stored in the latch when the signal SR_out2 [[1]] generated from the horizontal shift register 222 turns off. When the signal SR_out2 [[1]] generated from the

horizontal shift register 222 subsequently turns on, the digital signal SD (0) is input to the compactor. After being compared with the reference voltage, the digital signal “0” is stored in the latch when the signal SR_out2 [[1]] then generated from the horizontal shift register 222 turns off. When the signal SR_out2 [[1]] generated from the horizontal shift register 222 turns on, the digital signal SD (1) is input to the compactor. After comparison with the reference voltage, the digital signal “1” is stored in the latch when the signal SR_out2 [[1]] generated from the horizontal shift register 222 turns off. When the signal SR_out2 [[1]] then generated from the horizontal shift register 222 turns on, the digital signal SD (1) is input to the compactor. After comparison with the reference voltage, the digital signal “1” is stored in the latch when the signal SR_out2 [[1]] generated from the horizontal shift register 222 turns off.